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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,825	10/29/2003	Hiroyuki Ikeda	501.43187X00	6784
20457	7590	12/30/2005	EXAMINER	
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-3873			LIN, SUN J	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

sf

Office Action Summary

Application No.

10/694,825

Applicant(s)

IKEDA ET AL.

Examiner

Sun J. Lin

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2003 and 06 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-16 is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/29/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to Preliminary Amendment filed on 01/06/2004 regarding patent application 10/694,825 filed on 10/29/2003. Claims 17 – 27 have been cancelled. Claims 1 – 16 remain pending in the application.

QUAYLE ACTION

2. This application is in condition for allowance except for the following formal matters:

Claim Objections

- Claim 1, line 2, before "steps" delete ~~the~~.
- Claim 1, line 5, change "plural" to ~~plurality of~~.
- Claim 1, line 6, before "supply" delete ~~the~~.
- Claim 1, line 7, change "plural" to ~~plurality of~~.
- Claim 1, line 8, before "operation" delete ~~the~~.
- Claim 1, line 10, change "plural" to ~~plurality of~~.
- Claim 1, line 11, before "function" delete ~~the~~.
- Claim 1, line 13, change "plural" to ~~plurality of~~.
- Claim 2, line 1, change "respective" to ~~each of~~.
- Claim 2, line 2, change "plural" to ~~plurality of~~.
- Claim 2, line 4, after "type" insert ~~is~~.
- Claim 2, line 6, change "a second wiring" to ~~one wiring~~.
- Claim 2, line 6 – 7, change "a second wiring" to ~~another wiring~~.
- Claim 5, line 1, change "plural" to ~~plurality of~~.
- Claim 6, line 3, change "plural" to ~~plurality of~~.
- Claim 6, line 4, change "plural" to ~~plurality of~~.
- Claim 7, line 2, before "steps" delete ~~the~~.
- Claim 7, line 5, change "plural" to ~~plurality of~~.
- Claim 7, line 6, before "supply" delete ~~the~~.
- Claim 7, line 7, change "plural" to ~~plurality of~~.
- Claim 7, line 7 – 8, before "operation" delete ~~the~~.
- Claim 7, line 11, change "plural" to ~~plurality of~~.
- Claim 7, line 12, before "function" delete ~~the~~.
- Claim 7, line 13, change "the point" to ~~a point~~.

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Claim 7, line 15, change "plural" to **—plurality of—**.
Claim 9, line 2, before "steps" delete **—the—**.
Claim 9, line 6, change "plural" to **—plurality of—**.
Claim 9, line 6, before "supply" delete **—the—**.
Claim 9, line 8, change "plural" to **—plurality of—**.
Claim 9, line 12, before "operation" delete **—the—**.
Claim 9, line 15 (2 places), change "plural" to **—plurality of—**.
Claim 9, line 16, before "function" delete **—the—**.
Claim 9, line 18, change "plural" to **—plurality of—**.
Claim 9, line 19, change "plural" to **—plurality of—**.
Claim 11, line 2, before "steps" delete **—the—**.
Claim 11, line 5, change "plural" to **—plurality of—**.
Claim 11, line 6, before "supply" delete **—the—**.
Claim 11, line 7, change "plural" to **—plurality of—**.
Claim 11, line 8, before "operation" delete **—the—**.
Claim 11, line 10, change "plural" to **—plurality of—**.
Claim 11, line 12 change "plural" to **—plurality of—**.
Claim 11, line 14, change "plural" to **—plurality of—**.
Claim 11, line 15, before "function" delete **—the—**.
Claim 12, line 2, before "steps" delete **—the—**.
Claim 12, line 5, change "plural" to **—plurality of—**.
Claim 12, line 6, before "supply" delete **—the—**.
Claim 12, line 7, change "plural" to **—plurality of—**.
Claim 12, line 8, before "operation" delete **—the—**.
Claim 12, line 10, change "plural" to **—plurality of—**.
Claim 12, line 12, change "plural" to **—plurality of—**.
Claim 12, line 14, change "plural" to **—plurality of—**.
Claim 12, line 15, before "function" delete **—the—**.
Claim 14, line 2, before "steps" delete **—the—**.
Claim 14, line 5, change "plural" to **—plurality of—**.
Claim 14, line 6, before "supply" delete **—the—**.
Claim 14, line 7, change "plural" to **—plurality of—**.
Claim 14, line 8, before "operation" delete **—the—**.
Claim 14, line 10, change "plural" to **—plurality of—**.
Claim 14, line 11, before "function" delete **—the—**.
Claim 14, line 14, change "plural" to **—plurality of—**.

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- Claim 16, line 2, before "steps" delete ~~the~~.
- Claim 16, line 5, change "plural" to ~~plurality of~~.
- Claim 16, line 5, before "supply" delete ~~the~~.
- Claim 16, line 6, before "circuit portions" insert ~~plurality of~~.
- Claim 16, line 7, before "operations" delete ~~the~~.
- Claim 16, line 7, change "plural" to ~~plurality of~~.
- Claim 16, line 9, change "the power supply switch" to ~~a power supply switch~~.
- Claim 16, line 9, change "the always" to ~~a always~~.
- Claim 16, line 10, change "plural" to ~~plurality of~~.

Appropriate corrections are required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

Claims 1 – 16 are allowed because the prior art does not teach or fairly suggest the following subject matter:

- A method of manufacturing a semiconductor device comprising a step of invalidating function of a switch, which was performing switching between supply and non-supply of a first potential corresponding to a power supply potential to each of semiconductor substrate areas of a plurality of circuit cells in the semiconductor device, and connecting a second wiring, which supplies a signal for controlling operation of the switch, and a third wiring to a first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of circuit cells is fixed to the power supply potential in combination with other limitations as recited in independent **Claim 1**;
- A method of manufacturing a semiconductor device comprising a step of invalidating function of a switch, which was performing switching between

supply and non-supply of a first potential corresponding to a power supply potential to each of semiconductor substrate areas of a plurality of circuit cells in the semiconductor device, and connecting a second wiring, which supplies a signal for controlling operation of the switch, at a point intersecting a first wiring and connecting a third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of circuit cells is fixed to the power supply potential in combination with other limitations as recited in independent **Claim 7**;

- A method of manufacturing a semiconductor device comprising a step of invalidating functions of a first switch and a second switch, and connecting a second wiring, which supplies a signal for controlling operation of the first switch and the second switch, and a third wiring to a first wiring such that the potential supplied to each of semiconductor substrate areas of a plurality of circuit cells in an internal circuit area and a plurality of input/output circuit cells around the internal circuit area is fixed to a power supply potential in combination with other limitations as recited in independent **Claim 9**;
- A method of manufacturing a semiconductor device comprising a step of invalidating function of a switch, which was performing switching between supply and non-supply of a first potential corresponding to a power supply potential to each of semiconductor substrate areas of a plurality of circuit cells in the semiconductor device, with respect to a first circuit cell group, and connecting a second wiring, which supplies a signal for controlling operation of the switch, and a third wiring connected to the first circuit cell group to a first wiring such that the potential supplied to each of the semiconductor substrate areas of the first circuit cell group is fixed to the power supply potential in combination with other limitations as recited in independent **Claim 11**;
- A method of manufacturing a semiconductor device comprising a step of invalidating function of a switch, which was performing switching between supply and non-supply of a first potential corresponding to a power supply potential to each of semiconductor substrate areas of a plurality of field effect transistors in the semiconductor device, with respect to a first field effect transistor group, and connecting a second wiring, which supplies a signal for controlling operation of the switch, and a third wiring connected to the first

field effect transistor group to a first wiring such that the potential supplied to each of the semiconductor substrate areas of the first field transistor group is fixed to the power supply potential in combination with other limitations as recited in independent **Claim 12**;

- A method of manufacturing a semiconductor device comprising a step of invalidating function of a switch, which was performing switching between supply and non-supply of a first potential corresponding to a power supply potential to each of semiconductor substrate areas of a plurality of circuit cells in the semiconductor device, and disposing, instead of the switch, a connecting cell having information for connecting a second wiring, which supplies a signal for controlling operation of the switch, and a third wiring to a first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of circuit cells is fixed to the power supply potential in combination with other limitations as recited in independent **Claim 14**;
- A method of manufacturing a semiconductor device comprising steps of separating a power supply switch connected to a always operation-desired circuit portion of a plurality circuit portions from a power supply switch means and fixing the input of the power supply switch connected to the always operation-desired circuit portion to a power supply potential in combination with other limitations as recited in independent **Claim 16**.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571- 273 - 8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
December 27, 2005

A handwritten signature in black ink, appearing to read "James Lin", with a stylized flourish at the end.